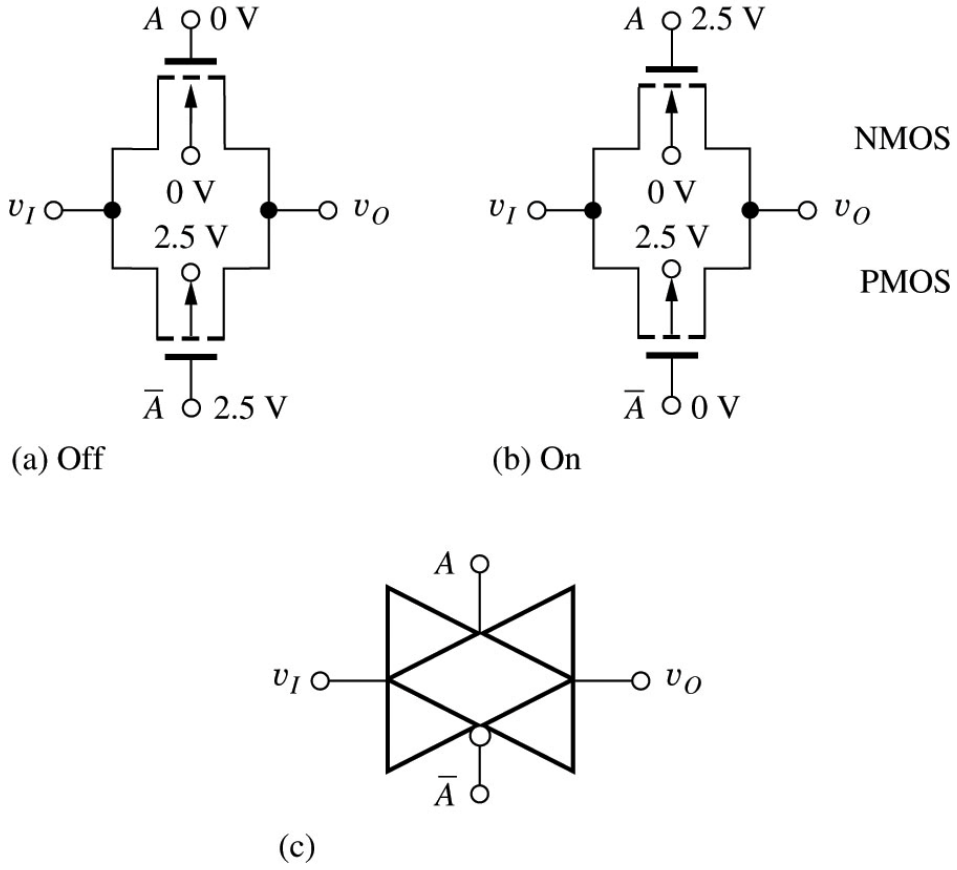
Announcements

- Homework #8 due Friday in class.
- Office hours today 2-3 pm and Th 12-1 pm
- Exam 2 regrade requests by in-class Friday.
- Grades online at catalyst.uw.edu/gradebook/dunham/86375

The CMOS Transmission Gate

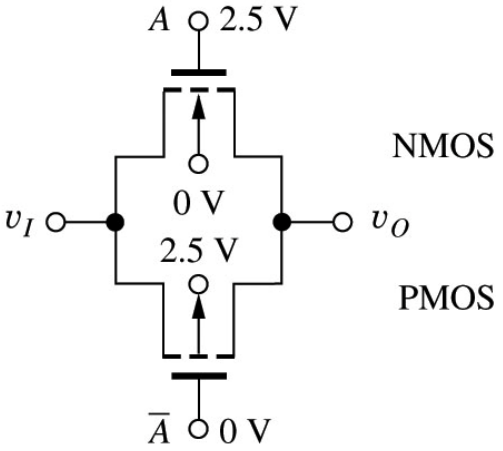
Bilateral Switch



- The CMOS transmission gate (T-gate) is a useful circuit for both analog and digital applications
- It acts as a switch that can operate up to V_{DD} and down to V_{SS}.
- Either side can be input/output.

The CMOS Transmission Gate

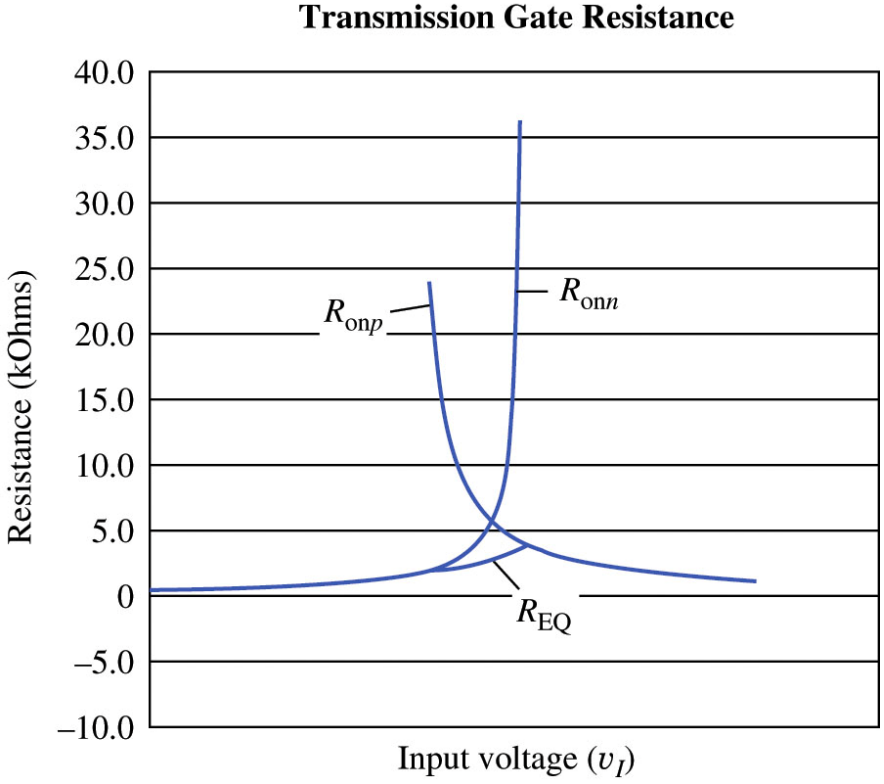
Equivalent On-Resistance



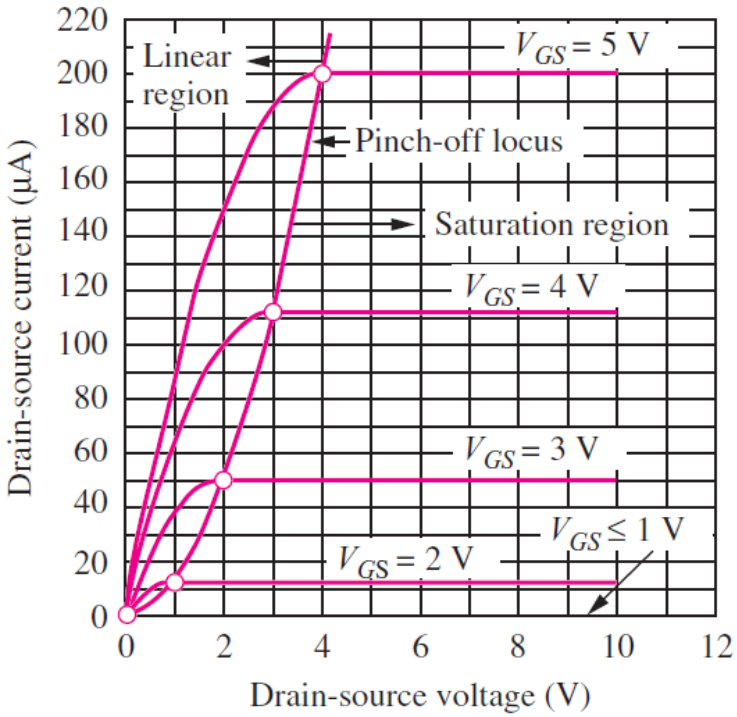
- Primary consideration is equivalent on-resistance which is given by the following expression:

$$R_{EQ} = \frac{R_{onp} R_{onn}}{R_{onp} + R_{onn}}$$

- NMOS conducts for $v_I < V_{DD} - V_{TN}$
- PMOS conducts for $v_I > -V_{TP}$



NMOS Output Characteristics
with Linearized Distributed Body Effect



Region	Current Equation	Condition
Cutoff	$i_D = 0$	$v_{GS} \leq V_{TN}$
Triode	$i_D = K_n \left(v_{GS} - V_{TN} - [1+\alpha]\frac{v_{DS}}{2}\right) v_{DS}$	$v_{GS} > V_{TN}$ $v_{GS} - V_{TN} > [1+\alpha] v_{DS}$
Satur-ation	$i_D = \frac{K_n}{2[1+\alpha]}(v_{GS} - V_{TN})^2$	$v_{GS} > V_{TN}$ $v_{GS} - V_{TN} \leq [1+\alpha] v_{DS}$

Transconductance (Saturation)

$$i_D = \frac{K_n'}{2(1+\alpha)}\frac{W}{L}(v_{GS} - V_{TN})^2$$

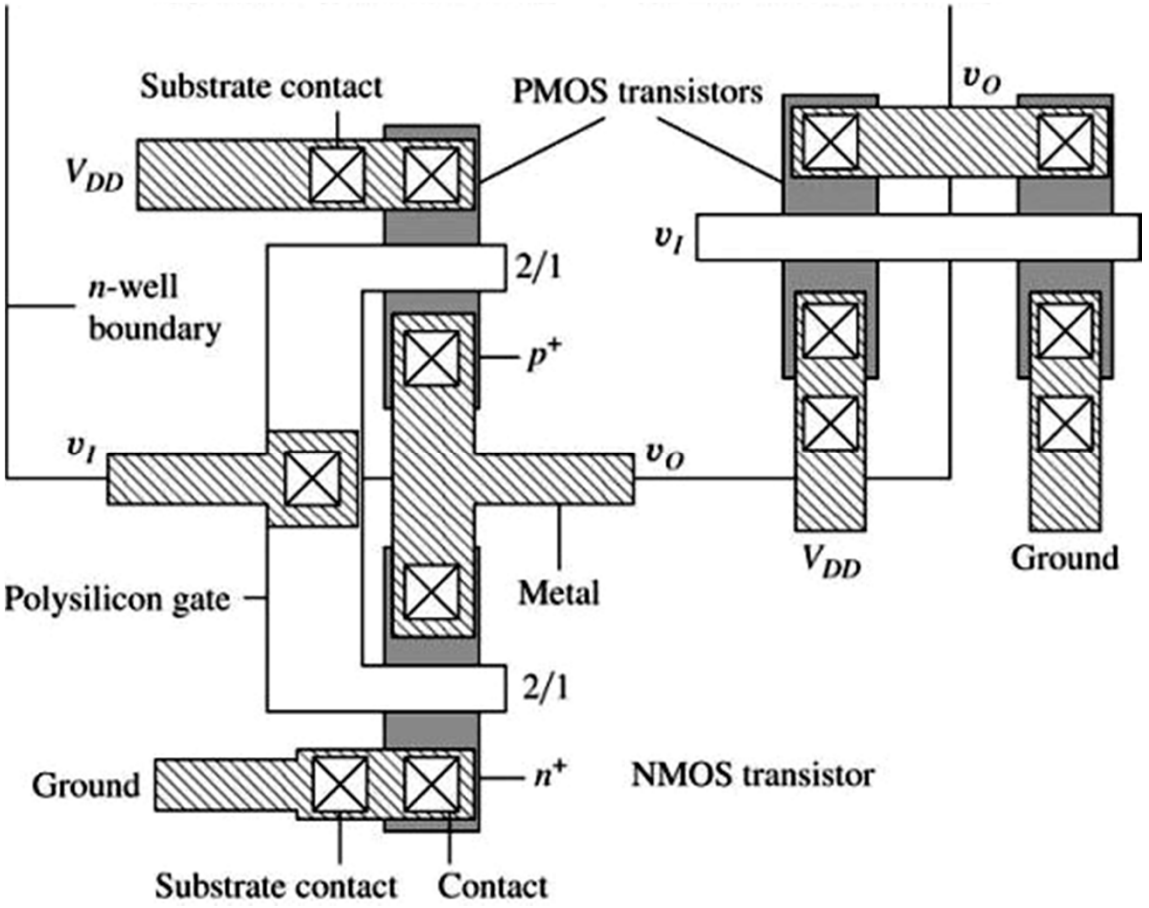
$$v_{\mathrm{DSAT}} = (v_{GS} - V_{TN})/[1+\alpha]$$

- Transconductance (change in i_D vs. change in v_{GS}):

$$g_m = \frac{di_D}{dv_{GS}} = K_n'\frac{W}{L(1+\alpha)}(v_{GS} - V_{TN})$$

CMOS Technology

Inverter Layout



- Two methods of laying out a CMOS inverter are shown
- The PMOS transistors lie within the n-well, whereas the NMOS transistors lie in the p-substrate
- Polysilicon is used to form common gate connections, and metal is used to tie the two drains together

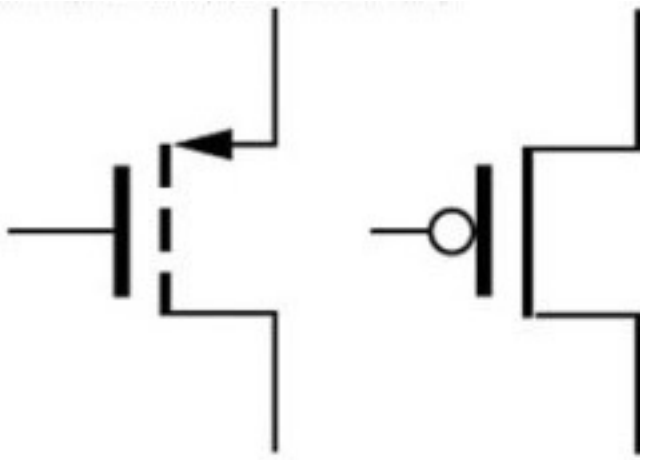
Minimum Size Gate

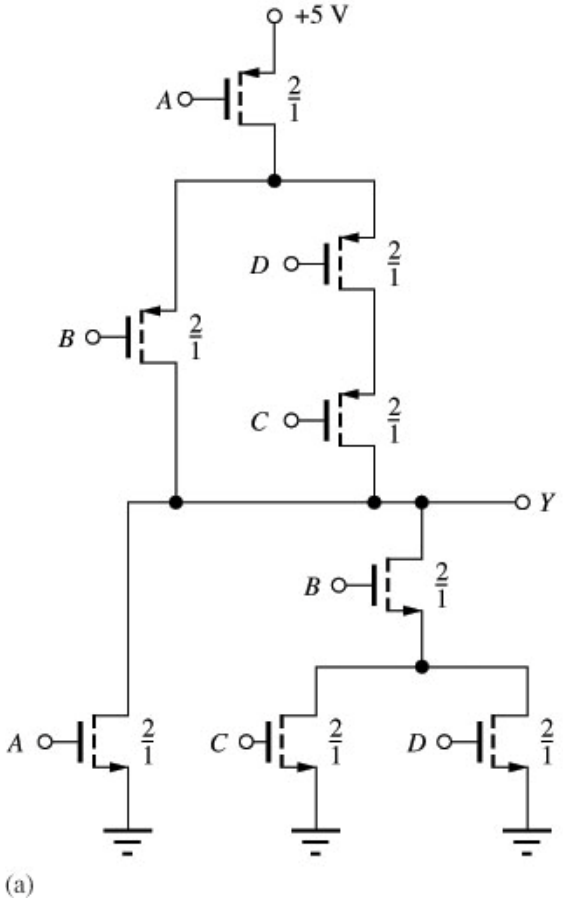
Design and Performance

- With CMOS technology, there is an area/delay tradeoff that needs to be considered

- If minimum feature sized are used for both devices, then the τ_{PLH} will be increased compared to the symmetrical reference inverter

Complex Gate Design





NMOS pull-down:

$$Y = \overline{A + B \cdot (C + D)}$$

$$= \bar{A} \cdot \left[\overline{B \cdot (C + D)}\right]$$

$$= \bar{A} \cdot \left[\bar{B} + \overline{(C + D)}\right]$$

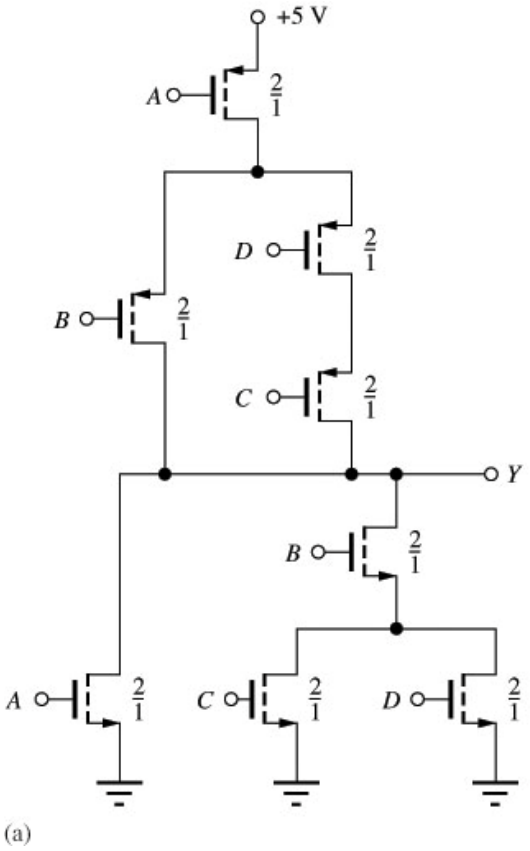
$$= \bar{A} \cdot [\bar{B} + \bar{C} \cdot \bar{D}]$$

which is PMOS pull-up circuit.

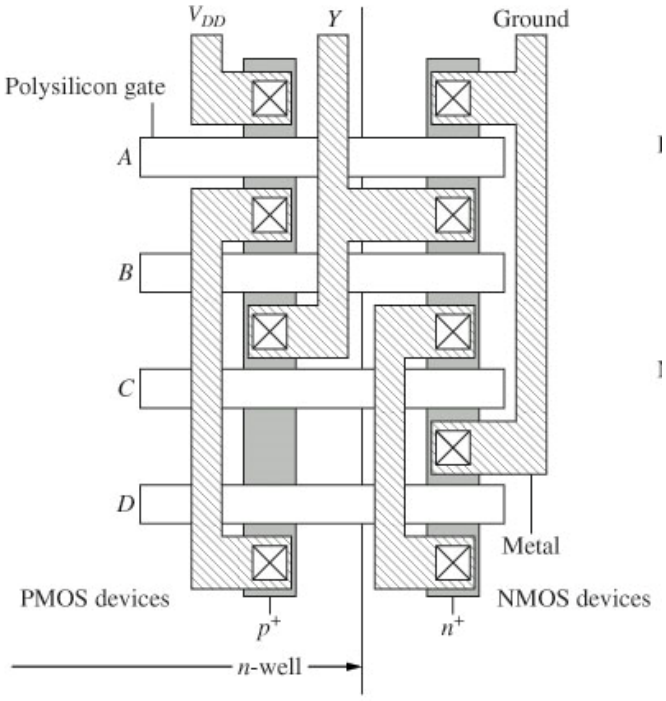
Minimum Size Complex Gate

Design and Layout

- The following shows the layout of a complex minimum size logic gate



(a)



(b)

